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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
HUBER, ROBERT T	

ART UNIT	PAPER NUMBER
2892	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/531,141	TRICOMI ET AL.	
	Examiner	Art Unit	
	ROBERT HUBER	2892	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *13 May 2008*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *2-9 and 13-17* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *2-9 and 13-17* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☒ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *11 April 2005* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☒ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Drawings

1. New corrected drawings in compliance with 37 CFR 1.121(d) are required in this application because the Applicant has not supplied separate drawings sheets with the application. The Examiner has referred to the drawings filed on April 11, 2005 in the document to which the application claims priority. Applicant is advised to employ the services of a competent patent draftsperson outside the Office, as the U.S. Patent and Trademark Office no longer prepares new drawings. The corrected drawings are required in reply to the Office action to avoid abandonment of the application. The requirement for corrected drawings will not be held in abeyance.

Claim Objections

2. Claims 2 – 8 and 13 – 15 are objected to because of the following informalities:

   a. The claims recite "the raised pedestals", however there is insufficient antecedent basis to support such a limitation. The independent claims 16 and 17, to which the dependent claims 2 - 8 and 13 - 15 depend upon, recite "stamped pedestals". Therefore, the examiner interprets the "raised pedestals" to refer to the "stamped pedestals."

   b. Claim 3 recites "the chip connection area", which lacks antecedent basis. Appropriate correction is required.

Claim Rejections - 35 USC § 112

3. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4. Claim 8 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Claim 8 currently depends on claim 1, however claim 1 has been canceled by the applicant. It is ambiguous to which claim that claim 8 currently depends on.

5. Claim 15 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Claim 15 currently depends on claim 11, however claim 11 has been canceled by the applicant. It is ambiguous to which claim that claim 15 currently depends on

Claim Rejections - 35 USC § 102

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

7. Claims 16, 2, 3, 6, and 7 are rejected under 35 U.S.C. 102(b) as being anticipated by Kwon et al. (US 5,365,409).

a. Regarding claim 16, **Kwon discloses an integrated circuit** (e.g. figure 5), **comprising:**

a semiconductor die (die 154);

a carrier device comprising a die paddle (paddle 152) **onto which the die is attached and a plurality of metallic leads** (leads 156) **each comprising an inner lead portion** (inner portion towards the die) **that extends to an outer lead portion** (inner portion towards the die), **where a plurality of stamped pedestals** (pedestals 158. regarding the term "stamped", this indicates a process of forming the pedestals. The patentability of a product does not depend on the method of its production. See MPEP 2113. The pedestals 158 may be formed by "stamping" the pattern from a larger sheet) **are arranged on the carrier device exteriorly surrounding and adjacent to the die paddle** (e.g. as seen in figure 5, the pedestals 158 exteriorly surround and are adjacent to the top of the die paddle 152);

a first bond wire extending from the die to a first of the plurality of stamped pedestals (bond wire 160), **and a second bond wire extending from the first of the plurality of stamped pedestals to an inner lead portion** (bond wire 162); **and**

a package that encapsulates the semiconductor die, the die paddle, the first and second bond wires and the inner lead portions (e.g. as seen in figure 5, there is a package, denoted by a dashed line, that encapsulates the die, paddle, wires and inner lead portions).

b. Regarding claim 2, **Kwon discloses the integrated circuit of claim 16, as cited above, wherein the raised pedestals have sidewalls with an angle (α) greater than 45 degrees with respect to a plane of the carrier device die paddle** (e.g. figure 5 shows the angle of the pedestal sidewall has an angle of 90 degrees with respect to the top or bottom plane of the die paddle 152).

c. Regarding claim 3, **Kwon discloses the integrated circuit of claim 16, as cited above, wherein the raised pedestals each have a plane surface which is parallel to a plane of the chip connection area** (e.g. as seen in figure 5, the top surface of the pedestal 158 is parallel to the plane area of the chip connection area 154) **and each has an area for connection of a single bonding** wire (e.g. as seen in figure 5, has an area for connecting a single bonding wire, e.g. wire 160).

d. Regarding claims 6 and 7, **Kwon discloses the structural limitations of the integrated circuit, as cited in claim 16. The process by which the raised pedestal is formed is not given patentable weight since the patentability of a product does not depend on the method of production. See MPEP 2113.**

Claim Rejections - 35 USC § 103

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

9. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

10. Claims 17, 4, 5, 9, 13, and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kwon.

a. Regarding claim 4, Kwon discloses the integrated circuit of claim 16, as cited above, but is silent with respect to explicitly stating that the height of each of the raised pedestals lies in the range between 1/10 and 1.5 times of a height of the semiconductor die. Kwon does show in Figure 5 that the height of the pedestal may be about 0.5 times the height of the die, but it is not explicitly stated.

It would have been obvious for one of ordinary skill in the art at the time the invention was made to modify the device of Kwon such that the pedestals are within the range of 1/10 to 1.5 times the height of the semiconductor die, since Kwon suggests through the figure this may be the case, and it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only ordinary skill in the art. *In re Aller*, 105 USPQ 233. One would have been motivated to make the height of the pedestal within the range of the chip in order to reduce lead length and stress on the leads.

b. Regarding claim 5, Kwon discloses the integrated circuit of claim 16, as cited above, but is silent with respect to a height of each of the raised pedestals lies in the range from 1/5 to twice a material thickness (h) of the carrier device. Kwon does show in Figure 5 that the height of the pedestal may be about 0.5 times the height of the carrier device, but it is not explicitly stated.

It would have been obvious for one of ordinary skill in the art at the time the invention was made to modify the device of Kwon such that the pedestals are within the range of 1/10 to 2 times the height of the carrier device, since Kwon suggests through the figure this may be the case, and it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only ordinary skill in the art. *In re Aller*, 105 USPQ 233. One would have been motivated to make the height of the

pedestal within the range of the carrier device in order to reduce lead length and stress on the leads.

c. Regarding claim 9, **Kwon discloses the integrated circuit of claim 16, as cited above, but is silent with respect to at least one unbonded raised pedestal on the carrier device** (e.g. figure 5 does not explicitly show that there is at least one unbounded pedestal). **However, Kwon does show in other embodiments that there may be at least one unbounded pedestal on the carrier device** (e.g. figure 4 shows that there may be both bonded and unbonded pedestals on the carrier device).

It would have been obvious for one of ordinary skill in the art at the time the invention was made to modify the embodiment of the device of Kwon shown in figure 5 such that there are unbonded pedestals, as shown in other embodiments of Kwon, since it is well-known in the art that circuit structures are dependent on the application of the device and may require that certain aspects of the circuit are not connected.

d. Regarding claim 17, **Kwon discloses an integrated circuit** (e.g. figure 5), **comprising:**

a semiconductor die (die 154);

a carrier device comprising a planar surface onto which the die is attached (planar surface of paddle 152) **and a plurality of metallic leads** (leads

156) **each comprising an inner lead portion** (inner portion towards the die) **that extends to an outer lead portion** (inner portion towards the die), where a **plurality of stamped pedestals** (pedestals 158. regarding the term "stamped", this indicates a process of forming the pedestals. The patentability of a product does not depend on the method of its production. See MPEP 2113. The pedestals 158 may be formed by "stamping" the pattern from a larger sheet) **are arranged on the carrier device exteriorly surrounding and adjacent to the planar surface** (e.g. as seen in figure 5, the pedestals 158 exteriorly surround and are adjacent to the top of the die paddle 152); **and**

a first bond wire extending from the die to a first of the plurality of stamped pedestals (bond wire 160), **and a second bond wire extending from the first of the plurality of stamped pedestals to an inner lead portion** (bond wire 162).

Kwon is silent with respect to explicitly stating that the carrier device is "metallic". However, Kwon discloses that the die paddle 152 of figure 5 may be formed of a ceramic (col. 6, line 53), **and that the die paddle 102 of figure 3 maybe formed of a ceramic comprising alumina nitride or beryllium oxide** (col. 5, lines 61 - 63). **Both alumina nitride and beryllium oxide are compounds made of metals.**

It would have been obvious for one of ordinary skill in the art at the time the invention was made to use a metallic material in the carrier device of Kwon since Kwon discloses in various embodiments that the carrier device may

comprise parts comprising metals. Furthermore, it has been held by the courts that selection of a prior art material on the basis of its suitability for its intended purpose is within the level of ordinary skill. *In re Leshin*, 125 USPQ 416 (CCPA 1960) and *Sinclair & Carroll Co. v. Interchemical Corp.*, 65 USPQ 297 (1945). One would have been motivated to make the carrier device metallic since metals are inexpensive and are easily manipulated to form both insulating portions (through oxidation of the metal) and conducting portions.

e. Regarding claim 13, **Kwon discloses the integrated circuit of claim 17, as cited above, where the raised pedestals make an angle (α) greater than 45 degrees with the plane of the carrier device at all sidewalls** (e.g. figure 5 shows the angle of the pedestal sidewalls have an angle of 90 degrees with respect to the top or bottom plane of the carrier device die paddle 152). **Kwon is silent with respect to explicitly stating the sides have rounded junctions parallel to the plane of the carrier device or being rounded as a whole.**

It would have been obvious for one of ordinary skill in the art at the time the invention was made to modify the device of Kwon such that the sides of the pedestals to have rounded junctions parallel to the plane of the carrier device or are rounded as a whole, since it has been held by the courts that a change in shape or configuration, without any criticality, is nothing more than one of numerous shapes that one of ordinary skill in the art will find obvious to provide based on the suitability for the intended final application. See *In re Dailey*, 149

USPQ 47 (CCPA 1976). It appears that the disclosed device of Kwon would perform equally well shaped as disclosed by the Applicant. One would have been motivated to have rounded pedestals since materials deposited often have rounded edges due to the formation process.

f. Regarding claim 14, Kwon discloses the integrated circuit of claim 17, as cited above, but is silent with respect to explicitly stating the height of the raised pedestals lies in the range between 1/10 of the die height and the die height itself Kwon does show in Figure 5 that the height of the pedestal may be about 0.5 times the height of the die, but it is not explicitly stated.

It would have been obvious for one of ordinary skill in the art at the time the invention was made to modify the device of Kwon such that the pedestals are within the range of 1/10 to the height of the semiconductor die itself, since Kwon suggests through the figure this may be the case, and it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only ordinary skill in the art. *In re Aller*, 105 USPQ 233. One would have been motivated to make the height of the pedestal within the range of the chip in order to reduce lead length and stress on the leads.

11. Claims 8 and 15 rejected under 35 U.S.C. 103(a) as being unpatentable over Kwon in view of Carter, Jr. et al. (US 6,365,976 B1).

a. Regarding claim 8, **Kwon discloses an integrated circuit, but is silent with respect to a silver or gold finish applied to the raised pedestals. Carter discloses that gold or silver finishes may be applied to raised pedestals in integrated circuits** (Col. 5, lines 18 - 22, disclose that the surface of the pedestals have a foil on them which may consist of silver or gold, or the pedestal may be covered with a tin-silver layer).

It would have been obvious for one of ordinary skill in the art at the time the invention was made to modify the device of Kwon such that there is a gold or silver finish on the raised pedestals since it was known in the art that such pedestals in integrated circuits my have a finish applied to them, as disclosed by Carter. One would have been motivated to have a gold or silver finish applied to the pedestals since gold and silver promote the bonding of the wires to the pedestals and are highly conductive.

b. Regarding claim 15, **Kwon discloses an integrated circuit, but is silent with respect to only in the areas of the raised pedestals, a finish, particularly silver or gold, is provided for bondability. Carter discloses that areas of pedestals may be provided with a gold or silver finish** (col. 5, lines 20 - 22, discloses that the pedestal ("dimple") may covered with a layer of tin-silver).

It would have been obvious for one of ordinary skill in the art at the time the invention was made to modify the device of Kwon such that there is a gold or silver finish on the raised pedestals since it was known in the art that such pedestals in integrated circuits my have a finish applied to them, as disclosed by Carter. One would have been motivated to have a gold or silver finish applied to the pedestals since gold and silver promote the bonding of the wires to the pedestals and are highly conductive.

Response to Arguments

12. Applicant's arguments with respect to claims 16 and 17 have been considered but are moot in view of the new ground(s) of rejection. The prior art of Kwon et al. either anticipates or is obvious over the claimed invention of claims 16 and 17. With respect to the applicants argument "where a plurality of stamped pedestals are arranged on the carrier device exteriorly surrounding and adjacent to the die paddle", the prior art of Kwon discloses the structure of this claimed limitation. The indication of the pedestals being "stamped" is a product-by-process limitation, and the patentability of a product does not depend on the method of its formation. See MPEP 2113. The pedestals could be formed by stamping them from a conducting sheet using a die to cut them to form.

Conclusion

13. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP

§ 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to ROBERT HUBER whose telephone number is (571)270-3899. The examiner can normally be reached on Monday - Thursday (9am - 6pm EST).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Thao Le can be reached on (571) 272-1708. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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July 7, 2008